



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,414	10/08/2003	Ebrahim Abedifard	400.241US01	7409
27073	7590	12/09/2005		
LEFFERT JAY & POLGLAZE, P.A. P.O. BOX 581009 MINNEAPOLIS, MN 55458-1009				
			EXAMINER LE, THONG QUOC	
			ART UNIT 2827	PAPER NUMBER

DATE MAILED: 12/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/681,414

Applicant(s)

ABEDIFARD, EBRAHIM

Examiner

Thong Q. Le

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 9-11 and 13-22 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 18-21 is/are allowed.
- 6) ☒ Claim(s) 9, 13, 16, 17 and 22 is/are rejected.
- 7) ☒ Claim(s) 10, 11, 14 and 15 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____

DETAILED ACTION

1. Amendment filed on 07/13/2005 has been entered.
2. Claims 9-11,13-22 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 9-11,13-22 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 9,13,16-17,22 are rejected under 35 U.S.C. 102(b) as being anticipated by Hara (U.S. Patent No. 5,406,521).

Regarding claims 9, 13, 16-17, 22, Hara discloses a flash memory device (Figure

1) comprising:

a plurality of n-wells comprising an n-type conductivity material (Figure 1, 2)
formed in a p-type substrate (Figure 1, 1);

a plurality of p-wells comprising a p-type conductivity material (Figure 1, 3), each
p-well located within an n-well;

a plurality of flash memory array blocks (Figure 2, 10), each comprising a
plurality of flash memory cells (Figure 2, MC) arranged in rows that are coupled together

by wordlines (Figure 2, WL), each flash memory array block located within a different p-well of the plurality of p-wells (Figure 2, p WELL3); and

a row decoder (figure 2, 11) coupled to the plurality of memory array blocks through the wordlines (Figure 2), external address signals (Figure 2, AR) coupled to the row decoder such that a wordline is selected in response to the address signals (Figure 2).

More specifically, Hara discloses wherein the first conductivity material is an n-type conductivity material (Figure 1, 2), and the second conductivity material is a p-type conductivity material (Figure 1, 1) as claims 16-17 disclosed, and a processor (Figure 2, 18) that controls operation of the electronic system and generates address signals as claim 22 disclosed.

6. Claims 9,13,16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Kawamura et al. (U.S. Patent No. 5,406,524).

Regarding claims 9, 13, 16-17 Kawamura et al. disclose a flash memory device (Figure 3) comprising:

a plurality of n-wells comprising an n-type conductivity material (Figure 3, N-WELL) formed in a p-type substrate (Figure 3, SUBSTRATE);

a plurality of p-wells comprising a p-type conductivity material (Figure 3, P-WELL), each p-well located within an n-well (Figure 3);

a plurality of flash memory array blocks (Figure 10, 171), each comprising a plurality of flash memory cells (Figure 10) arranged in rows that are coupled together by

wordlines (Column 9, lines 47-48), each flash memory array block located within a different p-well of the plurality of p-wells (Figure 23, Column 14, lines 1-7); and

a row decoder (Figure 10, 164) coupled to the plurality of memory array blocks through the wordlines (Column 9, lines 47-49), external address signals (Figure 10, addresses coupled to NAND gate of row decoder 164) coupled to the row decoder such that a wordline is selected in response to the address signals.

More specifically, Hara discloses wherein the first conductivity material is an n-type conductivity material and the second conductivity material is a p-type conductivity material (Column 14, lines 1-7) as claims 16-17 disclosed.

Allowable Subject Matter

7. Claims 10-11,14-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10-11,14-15 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Hara (U.S. Patent No. 5,406,521), Kawamura et al. (U.S. Patent No. 5,406,521), and others, does not teach the claimed invention having a voltage of 0V is applied to the n- well and a voltage of -5V is applied to the p-well of an unselected flash memory array block during an erase operation, and a voltage of 5V is applied to the n- well and a voltage of 5V is applied to the p-well of an unselected flash memory array block during a program operation as claims 10-11,14-15 disclosed.

8. Claims 18-21 are allowed.

Claims 18-21 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Hara (U.S. Patent No. 5,406,521), Kawamura et al. (U.S. Patent No. 5,406,521), and others, does not teach the claimed invention having a method for programming, and a method for erasing a memory array block of a plurality of memory array blocks as claims 19-21 disclosed.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Art Unit: 2827

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thong Q. Le
Primary Examiner
Art Unit 2827